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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,440	12/30/2003	Mark Yuk-Lun Wong	MWONG.102.US	1776

7590 05/01/2006

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EXAMINER	
SHANKAR, VIJAY	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,440	WONG ET AL.	
	Examiner	Art Unit	
	VIJAY SHANKAR	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Chin et al (5,581,778).

Regarding Claim 1, Chin et al teaches a MxN matrix display architecture comprising: MxN display devices (Col.13, lines 16-65); one video display controller (Fig.18) and one frame buffer (Figs.19-20), wherein only the one frame buffer and the one video display controller are required to control timing and flow of image data to the MxN display devices. (See Figs.20-27; Col.35, line 1- Col.42, line 40).

Regarding Claim 2, Chin et al teaches the display architecture wherein the one video display controller comprises: M line buffer systems for receiving image data from the frame buffer; N line fetching systems associated with each line buffer system for fetching and processing image data from its associated line buffer system and a data selector associated with each line buffer system for selecting the image data from one of the line fetching systems and sending the image data to one of the display devices. (See Figs.15,17-21; Col.35, line 60- Col.40, line 60).

Regarding Claims 3,7, Chin et al teaches the display architecture wherein each line buffer system comprises N line buffer segments storing image data to be sent to the line fetching systems. (See Figs.15,17-21; Col.35, line 60- Col.40, line 20).

Regarding Claims 4,8,9, Chin et al teaches the display architecture wherein each line fetching system comprises: a memory interface receiving image data from the frame buffer; a First-In-First-Out (FIFO) memory unit (Figs.17,18,20), and a scaler unit for scaling image data received from the FIFO memory unit or image data received from the line buffer system. (Col.10,line 43-53; Fig.17; Col.33, line 7- Col.34, line 45).

Regarding Claim 5, Chin et al teaches the display architecture further comprising a Time Division Multiplex Image Display (TDMID) algorithm for determining which line fetching system the data selector sends image data from and for controlling the timing for sending the image data. (See Figs.20-27; Col.35, line 1- Col.37, line 65).

Regarding Claim 6, Chin et al teaches the display architecture wherein the video display controller comprises: M line buffer systems; N line fetching systems associated with each line buffer system; N data selectors associated with each line buffer system (See Figs.15,17-21; Col.35, line 60- Col.40, line 60), and a Time Division Multiplex image Display (TDMID) algorithm for controlling the timing and data flow of the video display controller. (See Figs.20-27; Col.35, line 1- Col.37, line 65).

Regarding Claim 10, Chin et al teaches the MXN matrix display architecture comprising: MXN display devices (Col.13, lines 16-65); a frame buffer (Fig.19-20), and a video display controller (Fig.18) comprising M line buffer systems for receiving image data from the frame buffer, N line fetching systems associated with each fine buffer system for fetching and processing image data from its associated line buffer system, a data selector associated with each line buffer system for selecting the image data from one of the line fetching systems and sending the image data to one of the display devices (See Figs.15,17-21; Col.35, line 60- Col.40, line 60) and a Time Division Multiplex Image Display (TDMID) algorithm for controlling the timing and operation of the data selector, wherein only a single frame buffer and single video display controller combination are required to control timing and flow of image data to the MXN display devices. (See Figs.20-27; Col.35, line 1- Col.42, line 40).

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Inamori, Tanaka et al, Cahill,III teach the matrix display.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2629

VS